chipset **106** includes various bridge logic, peripheral logic and arbitration logic **107**, as described above with reference to FIG. **1**. The chipset **106** also includes mode logic **960** according to the present invention.

The bridge or chipset **106** couples through a memory bus **108** to main memory **110**. The main memory **110** is preferably DRAM (dynamic random access memory) or EDO (extended data out) memory, or other types of memory, as desired. The chipset logic **106** preferably includes a memory controller for interfacing to the main memory **110**.

The host/PCI/cache bridge or chipset **106** interfaces to a local expansion bus or system bus **120**. In the preferred embodiment, the local expansion bus **120** is the peripheral component interconnect (PCI) bus **120**. However, it is noted that other local buses may be used, such as the VESA (Video Electronics Standards Association) VL bus. Various types of devices may be connected to the PCI bus **120**. Expansion bus bridge logic **150** and an expansion bus **152** may also be coupled to the PCI bus **120**, as described above. As mentioned above, the mode logic **960** is operable to place the PCI bus **120** in either a normal PCI mode or in a real-time /multimedia mode optimized for multimedia transfers of periodic data.

The computer system shown in FIG. **21** optionally includes a real-time bus, also referred to as a multimedia bus **130**. The multimedia bus **130** preferably includes a 32 or 64 bit data path and may include address and control portions. The computer system shown in FIG. **21** may include a dedicated control channel, such as that shown in FIG. **7**, as desired. In the embodiment of FIG. **21**, the multimedia bus **130** is optionally provided to augment or supplement the PCI bus **120** when the PCI bus **120** is in multimedia mode.

One or more multimedia devices or multimedia devices **142**D, **144**D, and **146**D are coupled to each of the PCI bus **120** and the multimedia bus **130**. As shown in FIG. **22**, the multimedia devices **142**D–**146**D each include bus interface circuitry **962** which includes standard PCI interface circuitry **964** for interfacing to the PCI bus **120** when the PCI bus is in a normal PCI mode. The bus interface circuitry **962** also includes interface logic **966** for interfacing to the PCI bus **120** when the PCI bus **120** is in the multimedia mode. The bus interface circuitry **962** also includes interface logic **968** for interfacing to the optional multimedia bus **130**. The multimedia devices **142**D–**146**D may be any of various types of input/output devices, including multimedia devices and communication devices, as described above. The multimedia devices **142**D–**146**D are preferably similar to the multimedia devices **142**–**146** described above, except that the interface logic **962** in the multimedia devices **142**D–**146**D each include the interface logic for interfacing to the PCI bus **120** in multiple modes. As described above, the multimedia devices **142**D–**146**D may comprise video accelerator or graphics accelerator cards, video playback cards, MPEG decoder cards, sound cards, network interface cards, SCSI adapters for interfacing to various input/output devices, such as CD-ROMS and tape drives, or other devices as desired.

Thus, the multimedia devices **142**D–**146**D communicate with each other and with the CPU **102** and main memory **110** via the PCI bus **120**, as is well known in the art. The multimedia devices **142**D–**146**D also communicate data between using the PCI bus signal lines **120** when the PCI bus **120** is in the multimedia mode. As noted above, the real-time bus or multimedia bus **130** is optionally used to supplement the PCI bus **120** when the PCI bus **120** is in the multimedia mode.

In the preferred embodiment of the invention of FIG. **21**, the multimedia mode comprises placing the system bus or PCI bus **120** in a special mode optimized for real-time data transfers. In one embodiment of FIG. **21**, the special mode comprises a byte sliced mode which uses different byte lanes or channels of the PCI data lines for different types of multimedia transfers as described above. Thus, 16 bits of the PCI bus may be used for video transfers while the remaining 16 bits may be used for audio transfers simultaneously. Alternatively, the special mode comprises placing the PCI bus **120** in a timesliced or timeslotted mode as described above with reference to FIGS. **11** and **12**. Other types of multimedia modes may be used as desired.

C0NCLUSION

Therefore, the present invention comprises a novel computer system architecture which increases the performance of real-time applications. The computer system includes a PCI local bus and a real-time or multimedia bus. The multimedia bus may be used only for periodic data, and either the PCI bus or a separate control channel is used for addressing and control data. In one embodiment, the multimedia bus comprises two or separate channels for video, audio, and communications. A method is also disclosed which provides for improved performance of periodic data transfers on the multimedia bus. Distributed and centralized intelligence is also included in the various peripheral devices which provide for time slotting and improved data transfer performance.

Although the system and method of the present invention has been described in connection with the preferred embodiment, it is not intended to be limited to the specific form set forth herein, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents, as can be reasonably included within the spirit and scope of the invention as defined by the appended claims.

I claim:

1. A method for transferring periodic multimedia data on a bus in a computer system, wherein the computer comprises a CPU, main memory coupled to the CPU which stores data accessible by the CPU, bridge logic coupled to the CPU and the main memory, a bus coupled to the bridge logic which transfers multimedia data, and a plurality of multimedia devices coupled to the bus, the method comprising:

a first multimedia device generating addressing and control signals on the bus for a multimedia bus transfer, wherein the multimedia bus transfer is intended for a second multimedia device;

the first multimedia device generating one or more request signals on the bus for requesting that the multimedia bus transfer be a periodic multimedia data transfer;

the second multimedia device receiving the addressing and control signals on the bus for the multimedia bus transfer;

the second multimedia device receiving the one or more request signals;

the first multimedia device performing a plurality of multimedia bus transfers comprising periodic multimedia data transfers after the first multimedia device generating said addressing and control signals and said one or more request signals, wherein said plurality of multimedia data transfers comprise the first multimedia device transferring said periodic multimedia data on the bus to the second multimedia device, wherein said periodic multimedia data transfers are performed periodically on the bus, wherein said periodic multimedia data transfers do not require further control or handshaking signals prior to said periodic multimedia data transfers.